SUPPLEMENTAL INFORMATION CITED BY APPLICANTS THAT MAY BE MATERIAL TO THE PROSECUTION OF THE SUBJECT APPLICATION

Applicants: J.-S. Mok et al. Attorney Docket No.: LEPA122042

Application No.: 10/717,977 Art Unit: 2822 / Confirmation No.: 8002

Filed: November 20, 2003 Examiner: M.M. Trinh

Title: PARALLEL MULTI-LAYER PRINTED CIRCUIT BOARD HAVING IMPROVED INTERCONNECTION AND METHOD FOR MANUFACTURING THE SAME

U.S. PATENT DOCUMENTS

None.

FOREIGN PATENT DOCUMENTS

*Examiner Initial	Cite No.	Document No.	Kind Code	Publication Date (mm/dd/yyyy)	Country	English Abstract Provided	English Translation Provided
MT	F2	JP 02-288299		11/28/1990	JP	X	
MT	F3	JP 07-147464		06/06/1995	JP	X	
MT	F4	JP 10-224039		08/21/1998	JP	X	
MT	F5	JP 11-112118		04/23/1999	JP	X	
MT	F6	JP 2002-016358		01/18/2002	JP	X	
MT	F7	JP 2003-224339		08/08/2003	JP	X	

OTHER INFORMATION

None.

Examiner	**Date Considered**
/Michael Trinh/	01/11/2007

*Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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